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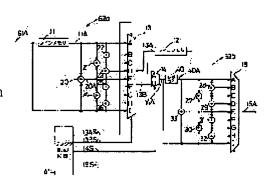
(54) DATA CONVERTING CIRCUIT

(57) Abstract:

PURPOSE: To enable the use of a low-speed memory, to reduce cost and to improve reliability by storing one piece of vertical interpolation data in a line memory and performing horizontal interpolation while alternately using the other vertical interpolation data and the data read from the line memory.

CONSTITUTION: The vertical interpolation is first performed by a vertical interpolation circuit 62a, one piece of data 13A of two kinds of vertical interpolation data are stored in a line memory 12, and the horizontal interpolation is performed by alternately using the vertical interpolation data recorded in this memory 12 and the other data outputted from the circuit 62a at a horizontal interpolation circuit 62b. Thus, since respective lines are interpolated with the data read out of the line memory 12, the line memory 12 just follows up data inputted for every one dot and does not require any high-speed operation. Therefore, the low-speed line memory can be used and a device can be provided at low cost.

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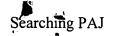
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